WHAT IS CLAIMED IS:

1. A failure analysis method comprising the steps of:

(a) irradiating a first light which includes a component whose wave length is 1 μm or more upon a semiconductor chip which is an object for an analysis from a front side;

(b) taking both a first wiring pattern image which is a reflected image of said semiconductor chip by said first light and a second wiring pattern image which is a transmission image of said semiconductor chip by said first light; and

(c) taking a light emission image of said semiconductor chip by a failure point from a back side of said semiconductor chip,

wherein both said second wiring pattern image and said light emission image are taken by an identical image pickup device.

2. The failure analysis method according to claim 1, further comprising the steps of:

(d) irradiating a second light which includes a component whose wave length is 1 μm or more upon said semiconductor chip from a back side; and

(e) taking both a third wiring pattern image which is a reflected image of said semiconductor chip by said second light and a fourth wiring pattern image which is a transmission image of said semiconductor chip by said second light,

wherein said third wiring pattern image is taken by said identical image pickup device.

3. A failure analysis method comprising the steps of:

(a) irradiating a laser beam for scanning which includes a component whose wave length is 1 μm or more upon a semiconductor chip which is an object for an analysis, and taking a first wiring pattern image which is a transmission image of said semiconductor chip by said laser beam and a second wiring pattern image which is a reflected image of said semiconductor chip by said laser beam; and

(b) taking an image of a failure point of said semiconductor chip,

wherein said step (a) is performed by a first image pickup device which is placed on a front side of said semiconductor chip and a second image pickup device which is placed on a back side of said semiconductor chip,

said step (b) is performed by a third image pickup device which is placed on the back side of said semiconductor chip, and

in advance of said steps (a) and (b), an alignment of said second image pickup device with said third image pickup device is performed.

4. The failure analysis method according to claim 3,

wherein said step (b) includes the step of;

(c) taking a light emission image of said semiconductor chip by a failure point from the back side of said semiconductor chip.

5. The failure analysis method according to claim 3,

wherein said step (b) includes the step of:

irradiating said laser beam upon said semiconductor chip from the back side, and taking the image of said failure point using an OBIC method or an OBIRCH method.

6. A failure analysis method comprising the steps of:

(a) irradiating a laser beam for scanning which includes a component whose wave length is 1 μm or more upon a semiconductor chip which is an object for an analysis, and taking a first wiring pattern image which is a transmission image of said semiconductor chip by said laser beam and a second wiring pattern image which is a reflected image of said semiconductor chip by said laser beam; and

(b) taking an image of a failure point of said semiconductor chip,

wherein said step (a) is performed by a first image pickup device which is placed on a front side of said semiconductor chip and a second image pickup device which is placed on a back side of said semiconductor chip, and

said step (b) is performed by said second image pickup device.